IN THE SPECIFICATION:

Please amend the second full paragraph appearing on page 2 as follows:

Current technology for metallization of an integrated circuit involves the forming of a conductive layer over the integrated circuit. A typical metallization process is one that is performed at the "back end of the ~~line"~~ line," which is after the formation of integrated circuits that are to be wired by the metallization process. A single conductive layer is often formed so that it is situated above the integrated circuit to be wired. After the conductive layer is formed, it is then patterned and etched into a shape of the desired wiring necessary to metallize the integrated circuit. Since the conductive layer is situated above the integrated circuit, the resultant metallization will also be above the integrated circuit in a ~~"wiring up"~~ "wiring-up" scheme.

Please amend the paragraph bridging pages 2 and 3 as follows:

Another type of metallization involves the formation of a conductive layer at least in part below the integrated circuit in a recess composed of an electrically insulative or dielectric material. Such a wiring scheme may be described as a ~~"wiring down"~~ "wiring-down" scheme. The recess can be either a trench, a hole, or a via. Depending upon the aspect ratio of the recess, poor step coverage of the conductive layer within the recess may result. Voids in the conductive layer within the recess may also result when the conductive layer does not completely fill up the recess. Voids and poor step coverage can cause the integrated circuit to experience an electrical failure. The electrical failure can be experienced during fabrication of the integrated circuit or after a period of time that the integrated circuit has been in use, such as where electrical contact with the conductive layer in the recess has been lost because the material of the conductive layer moves.

Please amend the first full paragraph appearing on page 4 as follows:

In accordance with the invention as embodied and broadly described herein, the present invention relates to ~~the~~ a method for manufacturing an interconnect structure situated on a semiconductor wafer having a substrate assembly thereon. A novel interconnect structure is also disclosed. The term ~~substrate assembly~~ "substrate assembly" is intended herein to mean a

substrate having one or more layers or structures formed thereon. As such, the substrate assembly may be, by way of example and not by way of limitation, a doped silicon semiconductor substrate typical of a semiconductor wafer.

Please amend the second full paragraph appearing on page 4 as follows:

The interconnect structure is formed in a dielectric material situated on the substrate assembly of the semiconductor wafer. The novel process forms the dielectric material into a recess having a specified ~~geometry~~ geometrical shape. The shape formed in the dielectric material will preferably be a recess therein. The recess can be a trench, a hole, a via, or a combination of a trench and a hole or via. The dielectric shape can be formed by processing the dielectric material by way of dry etching or other recess-creating process.

Please amend the paragraph bridging pages 4 and 5 as follows:

A seed layer is then formed upon the diffusion barrier layer. The seed layer helps to promote nucleation, deposition, and growth of a material that will be used to fill up the dielectric structure. The seed layer can also serve the purpose of increasing surface mobility of the diffusion barrier ~~layer~~ layer, which helps to make a desirable filling of the dielectric structure in the metallization process. Preferably, the material from which the seed layer is substantially composed is selected from the group consisting of ceramics, metallics, and intermetallics. More preferably, the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide. ~~Additionally~~ Additionally, and by comparison, the diffusion barrier layer will preferably be composed of a material having a melting point greater than or equal to that of the material from which the seed layer is ~~composed~~ composed.

Please amend the second full paragraph appearing on page 5 as follows:

An energy absorbing layer is then formed upon the conductor layer. The energy absorbing layer will preferably have a greater thermal absorption capacity than that of the electrically conductive layer. Alternatively, the energy absorbing layer will preferably ~~being~~ be

composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed. As another alternative, the energy absorbing layer will preferably be composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the electrically conductive layer is composed.

Please amend the second full paragraph appearing on page 7 as follows:

~~Figure~~ FIG. 1 is a partial cross-sectional elevation and perspective view of a dielectric material that is situated upon a monocrystalline silicon layer of a semiconductor wafer, the dielectric material having a dielectric structure formed therein that is shaped as a recess in the dielectric material, the recess featuring the combination of a hole extending to a trench in the dielectric material, the hole terminating at the monocrystalline silicon layer of the semiconductor wafer.

Please amend the third full paragraph appearing on page 7 as follows:

~~Figure~~ FIG. 2 is a partial perspective cross-sectional elevation view of a portion of ~~Figure~~ FIG. 1, showing various interconnect structure, including a trench in the dielectric material, a hole in the dielectric material, and a combination thereof, each ~~said~~ interconnect structure having thereon one or more layers of each of a barrier layer, a seed layer, a conductive layer, and an energy absorbing layer.

Please amend the first full paragraph appearing on page 8 and the section title directly preceding it as follows:

**DETAILED DESCRIPTION OF THE ~~PREFERRED EMBODIMENTS~~ INVENTION**

~~Figure~~ FIG. 1 depicts a semiconductor substrate assembly 10. A lower substrate known ~~as a~~ as silicon layer 22 is formed in semiconductor substrate assembly ~~10,~~ 10 and a dielectric material 14 is formed upon silicon layer 22. Lower substrate or silicon layer 22 defines a plane and comprises material selected from the group consisting of silicon dioxide, silicate ~~glass~~ glass, and mixtures or derivatives thereof. A hole 18 having a cylindrical shape extends from silicon

layer 22 to terminate at a trench 20 formed in dielectric material 14. Trench 20 is rectangular in cross-section.

Please amend the second full paragraph appearing on page 8 as follows:

~~Figure~~ FIG. 2 shows a cross-section 12 as seen ~~Figure~~ in FIG. 1. Another trench 32, and another hole 34 are also depicted. Trench 32 is not situated over a hole as is trench 20. ~~Figure~~ FIG. 2 also depicts a hole 34 having a triangular cross-section and extending from a top surface of dielectric material 14 to terminate at silicon layer 22. When ~~filed~~ filled with materials for a metallization process and subsequently planarized, holes 18, 34, and trenches 20, 32 become interconnect structures in the metallization process as described below.

Please amend the third full paragraph appearing on page 8 as follows:

To initiate the metallization process, dielectric material 14 is formed upon silicon layer 22 by conventional processing, such as depositing doped or undoped oxide by various CVD processes, or by TEOS deposition. Next, dielectric material 14 has recesses formed therein, ~~including for example~~ including, for example, holes 18, 34, and trenches 20, 32, the formation of which is by conventional processing methods such as patterning and etching.

Please amend the fourth full paragraph appearing on page 8 as follows:

After dielectric material 14 has been processed into the desired configuration of recesses, the next step is to form a barrier layer 24 ~~over the~~ over dielectric structure 16. Barrier layer 24 may be formed, by way of example and not by way of limitation, by multiple deposition of a material. The material from which barrier layer 24 is composed preferably will act as an adhesion layer for materials formed thereon, and also will ~~acts~~ act as a diffusion barrier to prevent the diffusion of material through barrier layer 24.

Please amend the paragraph bridging pages 9 and 10 as follows:

A seed layer 26 is formed over barrier layer 24 in the next step of the inventive method. The type of material used as seed layer 26 is dependant upon subsequent processing. If some

type of subsequent reflow process is needed for later added layers, or even a CVD process is going to be used for the formation of seed layer 26, seed layer 26 will preferably be formed prior to subsequent processing so as to clean barrier layer 24. The use of seed layer 26 provides a surface on barrier layer 24 that is substantially free of contaminates that may interfere with surface diffusion. Seed layer 26 promotes the deposition and growth of a layer of material that will be formed thereon. Additionally, seed layer 26 will preferably be the main conductor for current in the interconnect structure and will promote surface mobility of materials formed thereon so as to fill the recesses in dielectric material 14 ~~is a~~ in a desirable manner.

Please amend the first full paragraph appearing on page 10 as follows:

By way of example of materials and processes for formation of seed layer 26, a CVD tungsten process can be used. When so ~~processed~~ processed, there will be a nucleation of seed layer 26 that will be rich in both silicon and hydrogen, initially. The CVD tungsten process will then preferably undergo a chemistry change in the middle ~~thereof~~ thereof, so as to become rich in ~~hexflouride~~ hexafluoride such that a more pure form of tungsten material makes up seed layer 26. Those of ordinary skill in the art will understand the selection of proper seed layer 26 compositions, which selection may be done empirically by utilizing chemical potential differences and differences in diffusion characteristics of materials.

Please amend the second full paragraph appearing on page 10 as follows:

The seed layer may also be made of titanium nitride, which is preferred when aluminum is used in the interconnect structures. If so, the seed layer should be deposited in ~~situ~~ situ, prior to filling the interconnect structures with aluminum so as to enable the aluminum to freely flow and to avoid binding up the flow of the aluminum. Multiple layers can be used to make up the seed ~~layer, which~~ layer. The multiple layers will preferably be deposited in a vacuum system and will be composed of, for example, ~~of both~~ both titanium nitride and/or silicon.

Please amend the first full paragraph appearing on page 11 as follows:

When aluminum is used as conductor layer 28, the composition of barrier layer 24 will preferably be selected to avoid a heat induced reaction of the aluminum with the silicon in silicon layer 22 so as to form tetrahedrons in the silicon, ~~wherein by~~ whereby a detrimental effect is realized.

Please amend the second full paragraph appearing on page 11 as follows:

An energy absorbing layer 30 is then formed, preferably by deposition, upon conductor layer 28. Energy absorbing layer 30 retains thermal energy and comprises a material that has a ~~higher~~ lower thermal conductivity than conductor layer 28. By way of example and not limitation, if conductor layer 28 is composed of aluminum and energy absorbing layer 30 is composed of tungsten, the tungsten has a higher melting point ~~that~~ than aluminum. This results in the tungsten retaining more energy.

Please amend the third full paragraph appearing on page 11 as follows:

From a spectral point of view, if aluminum is used as conductor layer 28 and depending on how the aluminum layer is deposited, it is possible to obtain something that is not as spectrally reflective. A preferable characteristic of energy absorbing layer 30 is that it must be able to absorb more energy than the material that is used as conductor layer 28. The purpose behind this requirement is that when challenging structures ~~(e.g.~~ (e.g., recesses in dielectric material 14 having aspect ratios greater than four to one ~~(4/1))~~ (4:1)) are being formed ~~which~~ that are to be filled with a conductor, the conductor will flow more freely to fill a recess when thermal energy is retained within the conductor by a layer thereon that will better retain such thermal energy. As such, the ~~flowablility~~ flowability of the conductor is enhanced so that diffusion thereof into the recess is bettered.

Please amend the paragraph bridging pages 11 and 12 as follows:

Enhancing the diffusion characteristics of the material of the conductor is achieved by either volume diffusion or surface diffusion, each of which are time and temperature dependent.

The temperature of the conductor layer 28 is held high ~~for at~~ for a longer period of time while underlying or overlying materials retain thermal energy. The formation of energy absorbing layer 30 on conductor layer 28 substantially retains thermal energy under an interfacial surface of energy absorbing layer 30 so that the thermal energy can diffuse into conductor layer 28.

Please amend the first full paragraph appearing on page 12 as follows:

By way of example, if conductor layer 28 is aluminum, energy absorbing layer 30 can be titanium nitride, tungsten, or even a dielectric substance. A layer of titanium nitride is less thermally conductive than aluminum. If conductor layer 28 is copper, examples of energy absorbing ~~layers~~ layer 30 are tungsten, titanium nitride, tantalum or carbon.

Please amend the third full paragraph appearing on page 12 as follows:

A preferable step that follows the ~~forgoing~~ foregoing steps is the removal of materials from the semiconductor substrate assembly 10 by an abrasive planarizing process, for example, chemical mechanical planarizing. Material will be removed during the planarizing process until planarization line ~~36~~ 36, seen in ~~Figure~~ FIG. 2 as dashed lines, is reached. The resulting interconnect structures have been metallized so as to be buried within dielectric material ~~14, and as such~~ 14 and, as such, can be considered to be a metallization by "wire-down" technology. Subsequent and conventional processing can then following in the fabrication processing of the semiconductor substrate assembly 10.

Please amend the paragraph bridging pages 12 and 13 as follows:

~~Figure~~ FIG. 2 shows a novel dual ~~damescene~~ damascene structure depicted as hole 18 and trench 20 filled with each of barrier layer 24, seed layer 26, and conductor layer 28, where trench 20 has been planarized at planarization line 36. Planarization line 36 makes the metallization in an "inlaid" form. The two or "dual" metallization ~~damescene~~ damascene structure is seen in the inlaid combination of both hole 18 and trench 20.

Please amend the first full paragraph appearing on page 13 as follows:

The disclosed novel method is capable of desirable step coverage and being capable of filling in a recess within a dielectric material having an aspect ratio greater than about four ~~(4) to one (1).~~ to one (4:1). As such, the novel process improves both the yield and reliability over conventional processes.

Please amend the second full paragraph appearing on page 13 as follows:

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as ~~illustrated~~ illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.